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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,056	01/28/2004	Hiroaki Mochizuki	118328	9458

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EXAMINER	
NGO, HUYEN LE	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/765,056	MOCHIZUKI, HIROAKI	
	Examiner	Art Unit	
	Julie-Huyen L. Ngo	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 8-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 5, 2006 has been partially entered.

Response to Amendment

The amendment filed May 5, 2006 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material, which is not supported by the original disclosure, is as follows:

In the last clause of claims 1 and 2, ***"the second light shielding film and the gate electrode overlapping with each other in plan view by a distance of about 0.5 um".***

Applicant is to note that the disclosure (paragraph 0091) only describes that the distance L, which is the overlap portion of the gate electrode 203a and the light shielding film 11aP (fig. 8), is preferably about **0.5nm**.

Applicant is required to cancel the new matter in the reply to this Office Action.

Response to Arguments

Applicant's arguments with respect to the amended claims 1-5 and 8-11 in the Response filed on May 5, 2006 have been considered but they are not persuasive.

In response to applicant's argument that the reference of ***Hiroshi*** fails to show certain features of applicant's invention, it is noted that the features upon which applicant relies, i.e., ***"the second light shielding film and the gate electrode overlapping with each other in plan view by a distance of about 0.5 um"*** amended in claims 1 and 2 are not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-6 and 8-11 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

The last clauses of claims 1 and 2 contain subject matter, ***"the second light shielding film and the gate electrode overlapping with each other in plan view by a distance of about 0.5 um,"*** which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 3-6 and 8-11 are rejected as bearing the defects of claims 1 and 2 from which they depend.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 8-9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muraide Masao (JP2001-100251) in view of Hiroshi et al. (JP64-052129) provided in IDS.

With respect to the limitation amended in claims 1 and 2 regarding ***the second light shielding film and the gate electrode overlapping with each other in plan view by a distance of about 0.5 um***, which does not consistent with what being disclose in the disclosure as **0.5nm** (see paragraph 0091 and figure 8). For examination purpose, the Examiner interprets these claims in light of the specification and assumes that Applicant meant to recite 0.5nm instead of 0.5um.

Masao teaches (Figs. 1-10) forming an electro-optical device, comprising:

Claims 1, 2 and 11:

- a substrate 10 having an image display region and a peripheral region surrounding the image display region;
- a data line 6a;
- a scanning line 3a extending in a direction crossing the data line;

- a first switching element 30 disposed in the image display region, the first switching element being applied to a scanning signal is applied by the scanning line; and the first switching element including a semiconductor layer 1a having a source, drain and a channel;
- a pixel electrode 9a formed within the image display region, the pixel electrode being applied to an image signal is applied, by the data line, via the first switching element;
- a first light shielding film 11a formed in the image display region between the substrate and the first switching element, the first light shielding layer being in complete overlap with the source, the drain and the channel of the first switching element in plan view as shown in Fig. 8;
- a second switching element 103a to determine whether the image signal will be applied to the data line, the second switching element being located in the peripheral region, the second switching element including a semiconductor layer 1a having a source, drain region, a channel region, and gate electrode; the channel region being located between the source region and the drain region
- an interlayer insulating film 12, and
- a second light shielding film 53,formed in the peripheral region on an opposite side of the interlayer insulating film 12 from the second switching element 103a with the interlayer insulating film 12 there between, the second light shielding film 53 overlapping the source region and drain region of the second switching element in plan view, the second light shielding film 53 being divided into

separate sections with channel region of the second switching element as a boundary between the separate sections

However, Masao does not disclose that the second light shielding film overlapping the source region and drain region and a portion of the channel region of the second switching element in plan view, and ***the second light shielding film and the gate electrode overlapping with each other in plan view by a distance of about 0.5 nm.***

Hiroshi et al. teach (abstract and Figs. 1-2) forming the second light shielding film overlapping the source region and drain region and a portion of the channel region of the second switching element in plan view, and the second light shielding film 11 and the gate electrode 13 overlapping with each other in plan view by a distance of about 0.3 um for preventing direct fall of incident light from a gate side to an amorphous silicon layer (semiconductor layer of the switching element). Doing so would decrease the leak current between the drain and source, and increase in the parasitic capacity provision of the light-shielding layer is lessened.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify an electro-optical device as Masao disclosed with the second light shielding film overlapping the source region and drain region and a portion of the channel region of the second switching element in plan view; and with the second light shielding film overlapping the gate electrode in plan view by a distance of about 0.5 nm, which fall within the distance of < 0.3um, for preventing direct fall of incident light from a gate side to semiconductor layer of the switching element.

Doing so would decrease the leak current between the drain and source, and increase in the parasitic capacity provision of the light-shielding layer is lessened, as taught by Hiroshi et al.

The electro-optical device of Muraide Masao in view of Hiroshi et al. further comprising:

Claim 3:

- the second switching element having a laminated structure of a semiconductor layer, an insulating film, and an electrode film 115/5a, and the second light shielding film 53 overlapping at least a portion of the electrode film in plan view.

Claim 4:

- the electrode film 115/5a being formed in portions corresponding to the channel region

Claim 5:

- the sections of the second light shielding film and the electrode film being rectangular in plan view, and each section of the second light shielding film overlapping the electrode film in the long side of a rectangle in plan view.

Claim 6:

- the second switching element inherently being formed at the same time as the forming of the first switching element of the electro-optical device (paragraphs 18-20) since both switching elements are formed on the same semiconductor layer 1a, as shown in Figs. 8-10;

Claim 8:

- the second light shielding film being made of light shielding material (metal thin films Ti, Cr, W, Ta, Mo and Pb in paragraph 15).

Claim 9:

- the first light shield film 11a being formed to correspond to the data line and the scanning line in the image display region as shown in Fig. 3, the second light shielding member being formed at the same time as the first light shielding member (paragraph 28-29),

Claims 1-6 and 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murade Masao (US6330044B1) in view of Hiroshi et al. (JP64-052129) as provided in IDS.

With respect to the limitation amended in claims 1 and 2 regarding ***the second light shielding film and the gate electrode overlapping with each other in plan view by a distance of about 0.5 um***, which does not consistent with what being disclose in the disclosure as **0.5nm** (see paragraph 0091 and figure 8). For examination purpose, the Examiner interprets these claims in light of the specification and assumes that Applicant meant to recite 0.5nm instead of 0.5um.

Murade Masao teaches (Figs. 23-35) forming an electro-optical device, comprising:

Claims 1, 2 and 11:

- a substrate 10 having an image display region and a peripheral region surrounding the image display region;
- a data line 2;
- a scanning line 3 extending in a direction crossing the data line;
- a first switching element 102 disposed in the image display region, the first switching element being applied to a scanning signal is applied by the scanning line; and the first switching element including a semiconductor layer 1a having a source, drain and a channel;
- a pixel electrode 14 formed within the image display region, the pixel electrode being applied to an image signal is applied, by the data line, via the first switching element;
- a first light shielding film 7 formed in the image display region between the substrate and the first switching element, the first light shielding layer being overlap with the source, the drain and the channel of the first switching element in plan view as shown in Figs. 24-30;
- a second switching element to determine whether the image signal will be applied to the data line, the second switching element being located in the peripheral region, the second switching element including a semiconductor layer 1a having a source, drain and a channel;
- an interlayer insulating film 11,
- a second light shielding film 46, formed in the peripheral region on an opposite side of the interlayer insulating film 12 from the second switching element with

the interlayer insulating film 12 there between, the second light shielding film 53 overlapping the source region and drain region of the second switching element in plan view, the second light shielding film 46 being divided into separate sections with channel region of the second switching element as a boundary between the separate sections as shown in fig. 33,

However, Murade Masao fails to disclose that (a) the first light shielding layer being in complete overlap with the source, the drain and the channel of the first switching element in plan view; (b) the second light shielding film overlapping the source region and drain region and a portion of the channel region of the second switching element in plan view, and (c) that ***the second light shielding film and the gate electrode overlapping with each other in plan view by a distance of about 0.5 nm.***

Hiroshi et al. teach (abstract and Figs. 1-4) forming (a) the first light shielding layer being in complete overlap with the source, the drain and the channel of the first switching element in plan view for reducing leak current and the parasitic capacity; (b) the second light shielding film overlapping the source region and drain region and a portion of the channel region of the second switching element in plan view for reducing leaking current, and (c) the second light shielding film 11 and the gate electrode 13 overlapping with each other in plan view by a distance of about 0.3 um for preventing direct fall of incident light from a gate side to an amorphous silicon layer (semiconductor layer of the switching element). Doing so would decrease the leak current between the

drain and source, and increase in the parasitic capacity provision of the light-shielding layer is lessened.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify the electro-optical device as Murade disclosed with (a) the first light shielding layer being in complete overlap with the source, the drain and the channel of the first switching element in plan view for reducing leak current and the parasitic capacity; (b) the second light shielding film overlapping the source region and drain region and a portion of the channel region of the second switching element in plan view, and (c) with the second light shielding film overlapping the gate electrode in plan view by a distance of about 0.5 nm, which fall within the distance of < 0.3um, for preventing direct fall of incident light from a gate side to semiconductor layer of the switching element. Doing so would decrease the leak current between the drain and source, and increase in the parasitic capacity provision of the light-shielding layer is lessened in the device of Murade Masao, as taught by Hiroshi et al.

The electro-optical device of Murade Masao in view of Hiroshi et al. further comprising:

Claim 3:

- the second switching element 46 having a laminated structure of a semiconductor layer, an insulating film, and an electrode film 52/12/45, and the second light shielding film overlapping at least a portion of the electrode film in plan view.

Claim 4:

- the electrode film 45/48/49 being formed in portions corresponding to the channel region

Claim 5:

- the sections of the second light shielding film 46 and the electrode film being rectangular in plan view, and each section of the second light shielding film overlapping the electrode film in the long side of a rectangle in plan view.

Claim 6:

- the second switching element inherently being formed at the same time as the forming of the first switching element of the electro-optical device with same layer structures 7/11/12/13/15.

Claim 8:

- the light shielding film being made of light shielding material.

Claim 9:

- the first light shield film 7 being formed to correspond to the data line and the scanning line in the image display region,
- the second light shielding member 46 being formed at the same time as the first light shielding member 7,

Claim 10:

- the thickness of layer 11 is 1000 angstroms=100nm being less than 3000nm, thus the distance between the light shielding film and the second switching element being less than 3000 nm .

Contact Information

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Julie-Huyen L. Ngo whose telephone number is (571) 272-2295. The Examiner can normally be reached on M-Thursday.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Mr. David Nelms can be reached at (571) 272-1787.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 15, 2006

Julie -Huyen L. Ngo
Primary Examiner
Art Unit 2871